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Modulation of Surface Trap Induced Resistive Switching by Electrode Annealing in Individual PbS Micro/Nanowire-Based Devices for Resistance Random Access Memory

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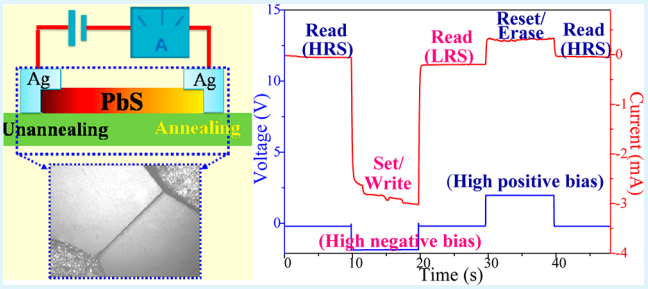
ABSTRACT: Bipolar resistive switching (RS) devices are commonly believed as a promising candidate for next generation nonvolatile resistance random access memory (RRAM). Here, two-terminal devices based on individual PbS micro/nanowires with Ag electrodes are constructed, whose electrical transport depends strongly on the abundant surface and bulk trap states in micro/nanostructures. The surface trap states can be filled/emptied effectively at negative/positive bias voltage, respectively, and the corresponding rise/fall of the Fermi level induces a variation in a degenerate/nondegenerate state, resulting in low/high resistance. Moreover, the filling/emptying of trap states can be utilized as RRAM. After annealing, the surface trap state can almost be eliminated completely; while most of the bulk trap states can still remain. In the devices unannealed and annealed at both ends, therefore, the symmetrical back-to-back Fowler−Nordheim tunneling with large ON/OFF resistance ratio and Poole−Frenkel emission with poor hysteresis can be observed under cyclic sweep voltage, respectively. However, a typical bipolar RS behavior can be observed effectively in the devices annealed at one end. The acquirement of bipolar RS and nonvolatile RRAM by the modulation of electrode annealing demonstrates the abundant trap states in micro/nanomaterials will be advantageous to the development of new type electronic components.



KEYWORDS: *PbS, resistive switching, nonvolatile resistance random access memory, surface and bulk trap states, modulation of trap states*

1. INTRODUCTION

Recently, the increasingly intelligent portable electronic products, such as Ipad and cellphone, put forward a great challenge to nonvolatile random access memory (RAM), display, and integrated circuits.[1,2] Therefore, the diverse RAM devices, like magnetron RAM (MRAM),[3] phase-change RAM (PCRAM),[4,5] ferroelectric RAM (FeRAM),[6] resistance RAM (RRAM),[7] and flash memory,[8] are widely discussed and investigated. However, the RRAM is one of the promising candidates for next-generation nonvolatile RAM, due to its simple cell structure, low operating voltage, fast operating speed, high endurance, high density, and nondestructive readout.[9−15] Resistive switching (RS) is an essential physical phenomenon in the RRAM and has been widely explored in numerous materials such as transition metal oxides,[16,17] organic polymer,[18] carbon nanotube,[19] p-n heterojunction,[20] and grapheme oxide film.[21] At present, some possible mechanisms like the formation/rupture of conducting filament,[22,23] Poole-Frenkel emission,[24,25] chemical oxidation and reduction process,[26] electronic hopping conduction,[27,28] and migration of oxygen vacancies[29,30] have been proposed to explain the origin of RS properties in various materials. However, the physicochemical processes at the micro/nanoscale remain controversial.[31,32] Therefore, the microscopic switching mechanisms still need to be explored and improved.

Owing to a narrow energy gap of 0.41 eV and a large exciton Bohr radius of 18 nm, PbS is an important semiconductor material with many eminent optical and electrical properties, which has extensively been applied in nonlinear optical devices, IR detectors, and display devices.[33−38] In the present study, individual PbS micro/nanowire-based two-terminal devices were constructed with Ag electrodes, and their RS and RRAM properties were investigated in detail. The electrical transport mechanism dominantly originates from the abundant trap states from Ag/PbS interface and PbS interior, which can be modulated effectively by annealing. Bipolar RS devices can be obtained by annealing one end electrode, and moreover, they can show a relatively low SET/RESET operating voltage. For RS, their filling/emptying of trap states can be effectively utilized as nonvolatile RRAM.

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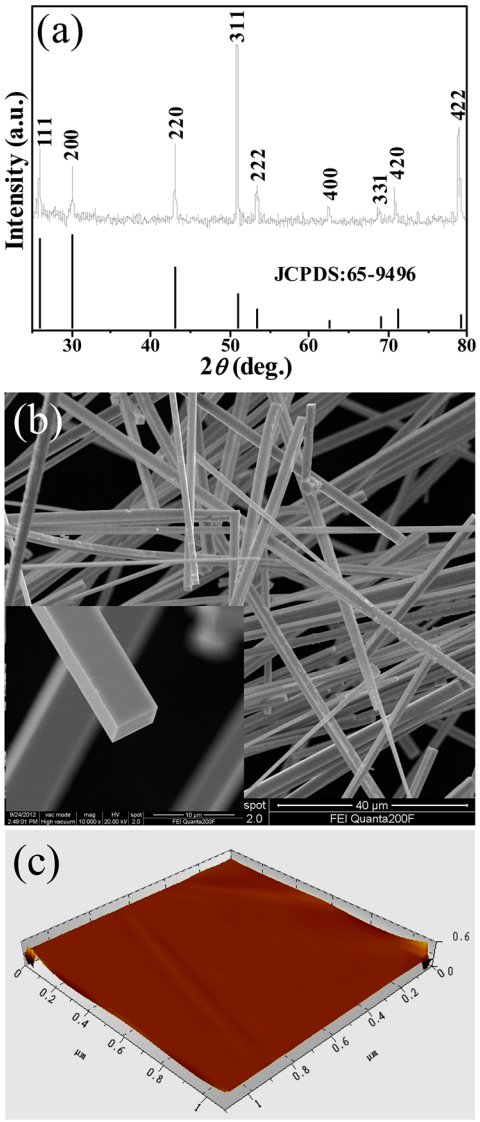

Figure 1. Characterization of as-prepared samples: (a) XRD pattern of, indexed to cubic PbS (JCPDS file: 65-9496); (b) a low-magnification FESEM image, showing the general morphology of as-prepared samples. The inset corresponds to higher magnification FESEM image, showing neat four prism structure; (c) AFM image, showing the relative smooth surface of the four prism structure.

2. EXPERIMENTAL METHODS

2.1. Synthesis of PbS Micro/Nanowires. PbS micro/nanowires were synthesized via a thermal evaporation of PbS powders which were prepared by a solvothermal reaction. First, lead nitrate, thiourea, and ethidene diamine (solvent) were mixed in a reaction kettle, then heated up to 200 °C, and maintained for 15 h. Through the above method, PbS powders were synthesized. Subsequently, a hollow horizontal alumina tube was installed inside a tubular furnace, the PbS powders were placed in an alumina crucible, and the catalyst was placed next to the PbS powders along the downstream side of flowing high-purity 95%N_2+5%H_2. Before heating, the tube was maintained at a constant flow of 200 mL/min for 1 h to ensure that O_2 was eliminated in the tube, and then the furnace was heated up to 1100 °C and held for 2 h. During the growth process, the gas flow was kept at a constant rate of 30 mL/min. After the reaction, the furnace was cooled down to room temperature, and PbS micro/nanowires were prepared successfully.

2.2. Characterization of Structure and Morphology. The resulting product was studied and analyzed by X-ray diffraction (XRD; Phillips X'Pert PRO with Cu Kα radiation), field-emission scanning electron microscopy (FESEM; FEI Quanta 200F), atomic force microscope (AFM; Agilent 5500), and X-ray photoelectron spectrometry (XPS; Thermo ESCALAB 250) to evaluate crystal structure and morphology.

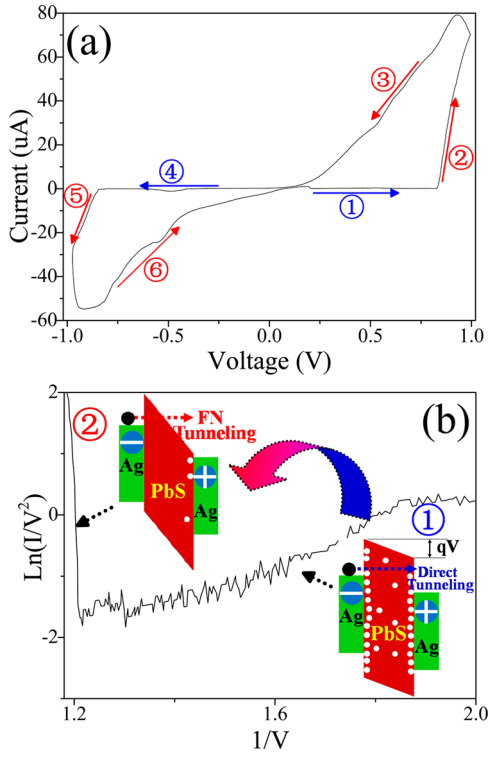

Figure 2. I–V characteristics of Ag/PbS/Ag device unannealed at both end electrodes. (a) I–V curve at a sweep voltage of ±1 V, showing that the current increases significantly at bias voltage higher than around ±0.84 V. The numbered arrows 1–6 indicate the direction of sweep voltage. (b) Plot of fitted curve for the steps 1 and 2 in (a) by FN tunneling mechanism. The insets correspond to the schematic diagram of direct tunneling (bottom) at low bias and FN tunneling (top) at high bias, respectively.

2.3. Fabrication and Performance Measurement of Devices. For the fabrication of devices, PbS micro/nanowires were dispersed on a flexible kapton insulating substrate, and the two-terminal Ag contacts of an individual wire device were fabricated by semidried silver paste under EPI optical microscope, and then, the postannealing of electrodes was carried out under N_2 atmosphere at 350 °C for 10 min. For the fabrication of devices annealed at one end, the unannealed electrode was fabricated after the other one was annealed. The electrical signal was measured by a synthesized function generator (Stanford Research System Model DS345) and a low-noise current preamplifier (Stanford Research System Model SR570). The electrical measurement was performed by a DC voltage sweep mode with the amplitude of 1 V and a frequency of 0.05 Hz at room temperature, and all the bias voltages were applied to the two end Ag electrodes. Additionally, all measurements were performed in the dark at room temperature.

3. RESULTS AND DISCUSSION

The XRD pattern (Figure 1a) of the as-synthesized product presents clear evidence that it is only composed of cubic PbS (JCPDS file: 65-9496). No characteristic peaks from other crystalline forms are detected in the XRD pattern. Low-magnification FESEM observation, as shown in Figure 1b, reveals that the as-prepared product consists of a great quantity of wire-like structures with typical lengths in the range of several to several tens of micrometers and widths in the range of hundreds of

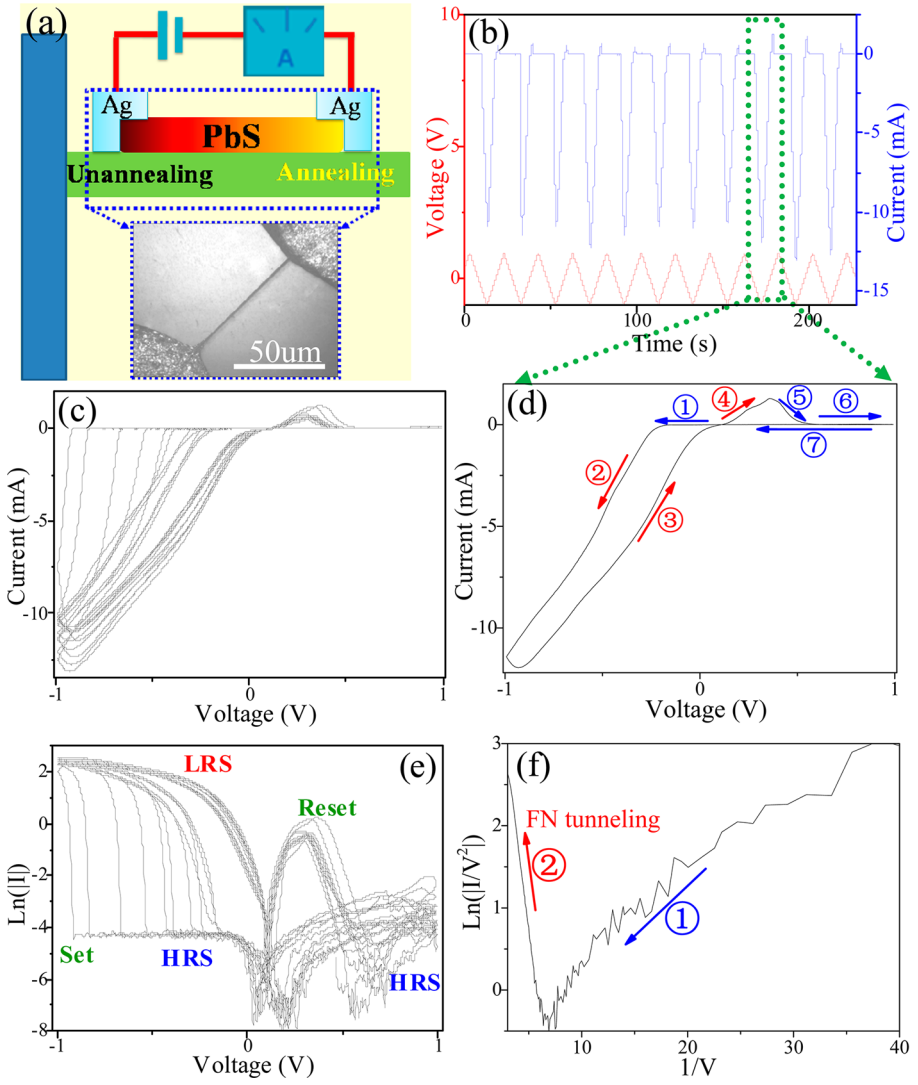

Figure 3. I–V characteristics of device annealed at one end electrode. (a) Schematic structure of the device and the scheme for electrical measurement, the inset is an optical image of a typical individual PbS wire-based device. (b) Plots of current response to a triangle wave voltage with an amplitude of 1 V and a frequency of 0.05 Hz. (c) Plots of 11 consecutive I–V cycles in linear scale, showing repeatability. (d) One I–V cycle plot in linear scale, related to green dotted frame in (b), indicating that current can increase abruptly (SET) at relatively high negative bias and then decrease abruptly (RESET) at relatively high positive bias. The numbered arrows 1–7 indicate the direction of sweep voltage. (e) Corresponding semilogarithmic scale in (d). (f) Plot of fitted curve for the steps 1 and 2 in (d) by the FN tunneling mechanism.

nanometers to several micrometers. These wires are randomly oriented, and most of them are straight. As seen from the higher magnification FESEM image, inset in Figure 1b, the neat four prism structures with a square cross section are clearly presented. Additionally, the higher magnification FESEM image and the AFM image (Figure 1c) show that the surface of the four prism structure is relatively smooth.

An individual PbS micro/nanowire was placed on a flexible insulated plastic substrate, and then the two-terminal device was fabricated by the contact of semidried silver with the two ends of the PbS micro/nanowire. For purposes of comparison, some devices were annealed at one end, and others were annealed at both ends. Figure 2a shows the typical I–V characteristics of the device unannealed at both ends of electrodes. It can be obviously seen that the device exhibits a symmetrical RS characteristic under cyclic sweep voltage of ±1 V. Moreover, the I–V curves show relatively large hysteresis loops, indicating the nonvolatile data storage capability.[39] At low positive bias, the current is extremely small and the device is almost nonconductive. With increasing positive or negative bias, the device current increases abruptly at about 0.84 V, and the resistance changes significantly from high resistance state (HRS) to low resistance state (LRS), namely RS effect. The resistance ratio of OFF to ON state is as high as about 380.

To gain more insight into the mechanism of the RS and electrical transport at different biases, the electrodes of devices were annealed at one or two ends, respectively. Figure 3 shows the I–V characteristics of the device annealed at one end. It can be seen that the I–V curves exhibit typical bipolar RS properties. When the unannealed electrode is subject to relatively low negative bias, the device is almost nonconductive. With increasing negative bias, however, the output current of the device increases abruptly with a threshold voltage of around 0.3–0.8 V, switching from HRS to LRS. Thus, a SET process occurs. Afterward, by sweeping the voltage from −1 to 0 V, the device current is still LRS (part 3). As the voltage is subsequently increased toward positive value (part 4), however, the device current remains the same low-resistance ON state.

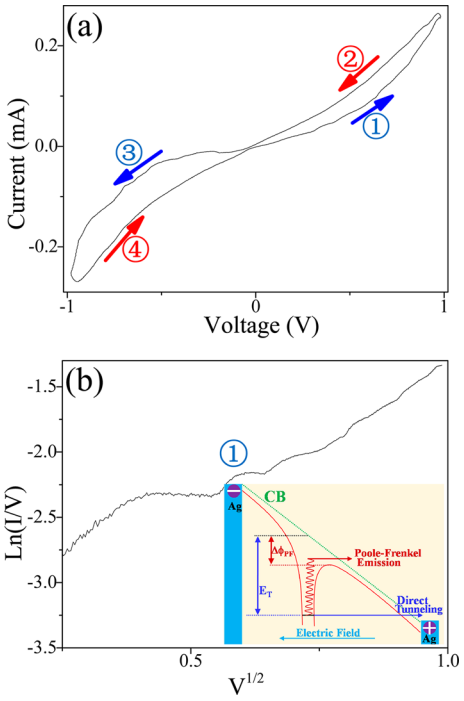

Figure 4. I–V characteristics of device annealed at both end electrodes. (a) I–V curve in linear scale, measured with a sweep voltage of ±1 V, displaying a closely symmetrical analog-type RS effect at negative and positive bias. The numbered arrows 1–4 indicate the direction of sweep voltage. (b) Fitted curve for step 1 in (a) by PF emission mechanism. The inset corresponds to the schematic diagram of PF emission from the traps inside PbS wire at an electric field.

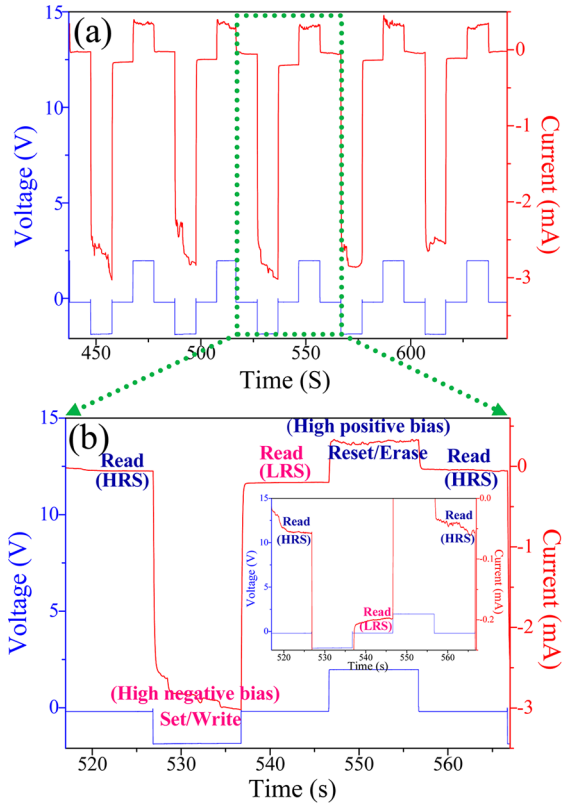

Figure 5. Write/read access of RRAM device annealed at one end, the red curve represents the current response, and the blue curve corresponds to the voltage applied at the unannealed end. (a) 5 consecutive cycles. (b) An enlargement of a green dotted frame in (a), and the inset corresponds to a higher magnification for LRS and HRS current, showing a detail programming/reading/erasing process. The information can be written after being applied a negative bias of −2 V at the unannealed electrode end, read out at a relatively low negative bias of −0.2 V, and erased/RESET after being applied a positive bias of 2 V.

When the bias voltage exceeds certain positive value of about 0.3 V, the device current decreases abruptly, showing an apparent negative differential resistance (NDR) feature. Correspondingly, the device is returned to the high-resistance OFF state, namely the RESET process. It can also be seen that the RS device can exhibit a relatively large memory window (R_{HRS}/R_{LRS}) and low operation voltage, indicating that it is easy to be further utilized as nonvolatile RRAM.

As seen from Figure 4, the current change of device, whose electrodes are annealed at both ends, is close to symmetry as well upon applying a cyclic sweep voltage. With increasing positive or negative bias, the current increases gradually rather than increases suddenly at a certain bias, forming an analog-type RS effect. Moreover, the I–V curves show relatively small hysteretic properties, indicating a poor nonvolatile data storage capability.

Due to the presence of relatively large hysteresis in the Ag/PbS/Ag devices unannealed or annealed at one end electrode, they exhibit great potential application in nonvolatile RRAM. Figure 5 shows the measurement results for the typical bipolar RS device annealed at one end electrode. The consecutive writing/reading/erasing processes are presented. As seen from the enlargement of a writing/reading/erasing/reading process, as shown in Figure 5b, the information can be programmed/written by applying a relatively high negative bias of −2 V at the unannealed electrode end, read out at relative low bias of −0.2 V, and reset/erased by applying a relatively high positive bias of 2 V at the unannealed electrode. After applying relatively high negative and positive forward bias at the unannealed electrode, the resistance difference in HRS and LRS is about 9.3 kΩ under reading out at −0.2 V. For the devices, unannealed at both ends, can also show rewritable memory effects, as shown in Figure 6. Moreover, they can similarly show rewritable memory effects when opposite operating bias voltages are applied. The symmetrical feature indicates that they should be back-to-back bipolar RS.

In order to further verify the presence of surface states in the PbS micro/nanostructures, XPS was measured, and the corresponding high resolution spectra of Pb 4f and S 2s are shown in Figure 7. The $4f_{5/2}$ and $4f_{7/2}$ of Pb are both composed of two peaks. As seen from the deconvoluted $4f_{5/2}$ and $4f_{7/2}$ peaks of Pb, blue peaks are much stronger than red ones, indicating that the content of unpassivated Pb atoms is higher. Therefore, it can firmly verify the presence of abundant surface states in the PbS micro/nanostructures.[40]

Since the work function of Ag (Φ_{Ag} = 4.26 eV) is lower than the electron affinity of PbS (χ_{PbS} = 4.6 eV),[41−43] it would be expected to form Ohmic contact when Ag electrode is in direct contact with type-n PbS. However, the Ag/PbS/Ag two-terminal devices are nearly nonconductive at low bias, especially for the unannealed devices. The results indicate that quantities of charge trap states exist in PbS, especially in vicinity of surface, which strongly affect the electrical transport of PbS-based devices. For the micro/nanostructured PbS with very large surface-to-volume ratio and sulfur vacancy-related n-type conduction, quantities of defects are present in their surface and

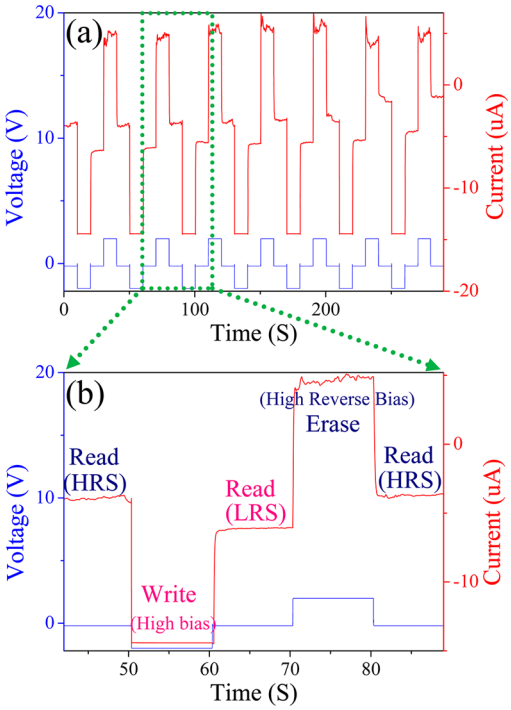

Figure 6. Write/read access of RRAM device unannealed at both end electrodes, the red curve represents the current response and the blue curve corresponds to the applied voltage. (a) 7 consecutive cycles. (b) An enlargement of a green dotted frame in (a), showing a detail programming/reading/erasing process. The information can be written after being applied a negative bias of −2 V at one end electrode, read out at a relatively low bias of −0.2 V, and erased/RESET after being applied a positive bias of 2 V.

interior. Especially for the dangling bonds from the breaking of lattice periodicity on their surface, they can induce acceptor-type surface states, and thus electrons will diffuse from wire interior toward its surface, resulting in band bending upward and the existence of carrier-depletion layer near the surface, where majority carriers (electrons) are almost depleted completely.[44−46] For the unannealed devices, the entire wires are almost depleted completely, and charges cross PbS wire through trapezoidal barrier. Therefore, the device is almost nonconductive. With increasing bias, the energy band bends gradually to become triangular. When the applied electric filed exceeds the barrier height, charges tunnel through the triangular barrier, which is analogous with field emission and Fowler−Nordheim (FN) tunneling occurs,[47,48] and the corresponding schematic diagrams of conduction mechanism are inset in Figure 2b. I−V curve near the current mutation is fitted based on the FN tunneling mechanism, and a linear decrease relation of $\ln(|I/V^2|)$ versus $|1/V|$ can be found when the applied bias exceeds the SET voltage, as illustrated in Figure 2b and 3f. Under FN tunneling at high bias, electrons can inject from the negative electrode into the surface traps, resulting in a filling of trap states. Accordingly, the concentration of free carriers increases due to the rise of the Fermi level. When the position of the Fermi level is higher than that of the PbS conduction band (CB), the degenerate semiconductor is formed in vicinity of the unannealed electrode, and an antiblocking layer is created at the Ag/PbS interface. Consequently, a conductive channel is created effectively, and the device is switched to LRS. Near the negative end, the change of PbS from a nondegenerate into a degenerate state corresponds to the SET process of RS. After that, when the unannealed electrode is subject to a relatively high positive bias, the surface trapped charges can be emptied effectively due to the electron injection from trap states into the positive electrode. Thus, the degenerate semiconductor is back to nondegenerate, and a blocking layer (depletion region) is created at the Ag/PbS interface. As a consequence, the device shows a NDR feature and simultaneously returns to HRS, namely, a RESET process. For the surface state-dependent RS, the transformation between a degenerate and a nondegenerate state is the predominant SET/RESET process. Upon annealing at the temperature above about 350 °C, sulfur can combine with Ag at the Ag/PbS interface, resulting in a dramatic reduction of surface trap state density.[49] As a consequence, the height and width of surface barrier decrease significantly, and it is very easy for charges to cross the Ag/PbS interface by thermionic emission. The surface traps are very abundant. For each sweep, it is very difficult for the filling of surface traps to maintain wholly consistent. Therefore, the SET point shows a difference, and it still remains a relatively small range of 0.3−0.8 V. The devices are strongly dependent on the surface states. For smaller size wires, their specific surface area is much larger, and, therefore, the entire wires are depleted, resulting in a nonconductive behavior. In addition, the trapped charges can be thermally excited, and the devices can turn to be nonconductive when the test temperature is higher than about 100 °C. Although the surface trap states can almost be eliminated completely after annealing, most of the bulk trap states can still remain within the PbS wires. For the devices annealed at both ends, therefore, the bulk trap-controlled emission is the dominant conduction mechanism rather than interface-controlled injection. Their corresponding

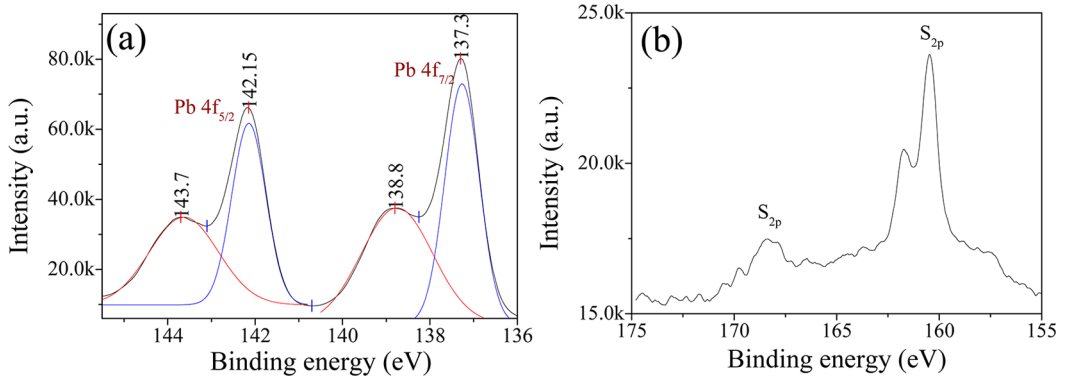

Figure 7. High resolution XPS spectra of Pb 4f (a) and S 2s (b). In (a), the red and blue lines are fitting curves and the black line is the sum of them.

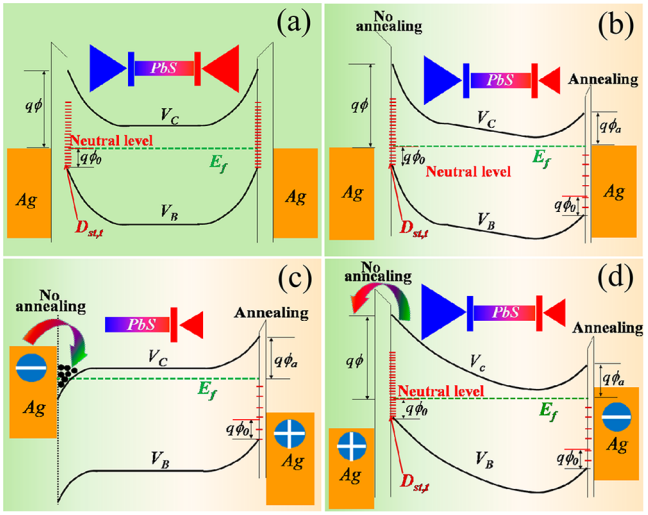

Figure 8. Schematic energy band diagram for illustrating the RRAM effect in the two-terminal Ag/PbS/Ag device. (a) Unannealed device, showing that the entire wire is completely depleted and Fermi level is pinned due to abundant surface trap states. (b) Annealed device at one end electrode (right), showing that the surface trap states is almost eliminated at the annealed Ag/PbS interface. (c) The unannealed end was subject to relatively high negative bias. Electrons are injected from negative electrode into surface traps, resulting in the formation of antiblocking layer at the annealed Ag/PbS interface. (d) The unannealed end was subject to relatively high positive bias. Electrons are injected from surface trap states into positive electrode, and then surface trap states are emptied, resulting in the formation of thicker blocking layer (depletion region) near the annealed Ag/PbS interface.

I–V curves can be fitted by Poole–Frenkel (P–F) emission mechanism,[50] which is an electric-field-enhanced thermal emission from a bulk trap state into a continuum of electronic state, and a linear relation of ln(I/V) versus $V^{1/2}$ is well achieved, especially at high electric field, as shown in Figure 4b. The current is relatively large at low bias, and moreover, it increases gradually rather than rises abruptly above a certain bias. For the conduction analysis above, the RS and nonvolatile RRAM mechanism in the modulated Ag/PbS/Ag devices could be illustrated in Figure 8.

4. CONCLUSIONS

In summary, abundant surface and bulk trap states exist in Ag/PbS interface and PbS interior, respectively, which strongly affect the electrical transport of Ag/PbS/Ag two-terminal micro/nanodevices. For the unannealed devices, the entire PbS wires are depleted completely due to quantities of surface and bulk trap states, and their Fermi levels are pinned. Therefore, the devices are almost nonconductive at relatively low bias. With increasing bias, the energy band bends gradually and varies from trapezoidal to triangular barrier, and simultaneously, the surface trap states can be filled up by the electrons from negative electrode, resulting in the rise of a Fermi level higher than CB. Thus, the conductive channels are created, and the devices change into LRS due to the formation of an antiblocking layer at the Ag/PbS interface. Subsequently, the surface trap states can be emptied after applying relatively high positive bias, and correspondingly, the devices are back to LRS. After annealing, the surface trap states can almost be eliminated completely, while most of the bulk trap states can still be remained. Under cyclic sweep voltage, therefore, the unannealed devices can show symmetric back-to-back FN tunneling conduction behavior. The devices annealed at both ends can show dominant PF emission conduction behavior, and the ones annealed at one end can show typical bipolar RS behavior. For the low-dimensional materials with abundant trap states, their effective and feasible modulation by external environments will be advantageous to the development of new type electronic components.

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Notes

The authors declare no competing financial interest.

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